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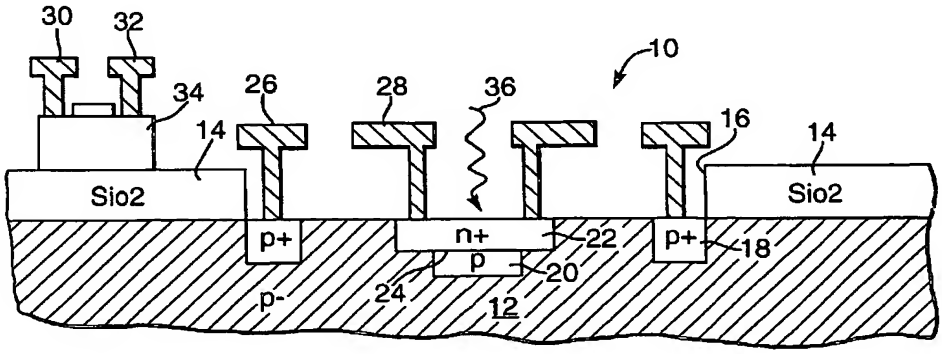
(54) Title: PHOTODETECTOR CIRCUITS



(57) Abstract: A photodetector circuit incorporates an APD detector structure (10) comprising a p- silicon handle wafer (12) on which a SiO_2 insulation layer (14) is deposited in known manner. During manufacture a circular opening (16) is formed through the insulation layer (14) by conventional photolithography and etching, and an annular p+ substrate contact ring (18) is implanted in the handle wafer (12) after opening of the window (16). The APD itself is formed by implantation of a p region (20) and an n+ region (22). After the various implantation steps a metallisation layer is applied, and annular metal contacts are formed by the application of suitable photolithography and etching steps, these contacts comprising an annular contact (26) constituting the negative terminal and connected to the p+ substrate contact ring (18), an annular metal contact (28) constituting the positive terminal and connected to the n+ region (22) of the APD, and source and drain contacts (30) and (32) (not shown in Figure 1) connected to the source and drain of one or more CMOS MOSFET devices of the associated CMOS readout circuitry fabricated within a Si layer (34) formed on top of the insulation layer (14). Such an arrangement overcomes the problem of combining APDs with CMOS circuits in that APDs operate at relatively high reverse bias (15-30V) and CMOS circuits operate at low voltage (SV), and the arrangement must be such as to prevent the high bias voltage from affecting the operation of adjacent CMOS transistors.

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